

AMENDMENT UNDER 37 C.F.R. § 1.111
Application Serial No. 10/791,381
Attorney Docket No. Q80213

AMENDMENTS TO THE DRAWINGS

Please remove Figure 1A and replace with Replacement Figure 1A.

Attachment: Replacement Sheet

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REMARKS

Upon entry of the present Amendment, claims 1-21 are all the claims pending in the application. Claims 6-13 are withdrawn from further consideration pursuant to the Response to Restriction Requirement, filed April 8, 2005. Claim 1 is amended, and new claims 14-21 are added. No new matter is presented.

To summarize the Office Action, the drawings and the specification are objected to for informalities, and claims 1-5 are rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Sultan et al. (U.S. Patent No. 6,063,682, hereinafter "Sultan"). The outstanding objections and rejections are addressed below.

Objection to the Drawings

The Examiner objected to the drawings because the lines from the first impurity diffusion region (5) and the second impurity diffusion region (6) in Figure 1A do not point to the proper elements. In response, Applicant submits herewith Replacement Figure 1A which identifies these elements consistent with the disclosure. Therefore, the Examiner is requested to enter Replacement Figure 1A and to withdraw the objection. Further, the Examiner is requested to indicate acceptance of the drawings in the next action.

Objection to the Specification

The Examiner objected to the specification for several grammatical errors. Applicant has amended the specification to correct the grammatical errors identified by the Examiner. Accordingly, the Examiner is requested to withdraw this objection.

Claim Rejections - 35 U.S.C. § 102

Claim 1 defines a novel semiconductor device presenting new features. For example, the semiconductor device is provided with a semiconductor substrate, a gate electrode formed on the substrate, and an impurity diffusion region formed beside the gate electrode with a PN junction with a region in the semiconductor substrate. Further, the impurity diffusion region comprises a first impurity diffusion region including a first P-type impurity and located in the proximity of a surface of the semiconductor substrate, and a second P-type impurity diffusion region located below the first impurity diffusion region and including a second P-type impurity having a smaller diffusion coefficient in the semiconductor substrate than the first P-type impurity. In addition, each of the first impurity diffusion region and the second impurity diffusion region form the PN junction with the region of the semiconductor substrate.

Notwithstanding the Examiner's rejection, Applicant submits that Sultan fails to teach or suggest all the features of claim 1. For instance, the semiconductor device defined by claim 1 requires that each of the first and second impurity diffusion region forms the PN junction with the region of the semiconductor substrate. In an exemplary embodiment, the source/drain region 4 is provided with the first impurity diffusion region (boron) and the second impurity diffusion region (indium). Thus, each of the first impurity diffusion region (boron) and the second impurity diffusion region (indium) forms the PN junction with the region of the semiconductor substrate. *See Specification at Figs. 1A and 7.*

However, Sultan fails to teach or suggest *at least* this feature. Rather, Sultan teaches that indium implanted into the n-well 34 does not make a PN junction. *See* Sultan at Fig. 1f. Further, according to Sultan, the boron implanted into the n-well 34 forms the lightly doped regions 78, 80 and boron makes the PN junction. *See* Sultan at Fig. 1f and col. 6, lines 44-47 and col. 7, lines 64 - col. 8, line 1. As a consequence, Sultan does not teach a PN junction formed by a first impurity diffusion region and a second impurity diffusion region.

Therefore, Sultan fails to teach or suggest all the features of claim 1, and reconsideration and withdrawal of the rejection of claim 1 is requested. Further, claims 2-5 are believed to be allowable at least by virtue of depending from claim 1. Accordingly, allowance of claims 1-5 is requested.

New Claims

In order to provide additional claim coverage merited by the scope of the invention, new claims 14-21 are added, with claims 14 and 18 being in independent form. These claims are believed to be allowable at least for the reasons discussed below.

Claim 14

Independent claim 14 defines a novel semiconductor device provided with a semiconductor substrate, a pair of lightly doped drain (LDD) regions formed apart from each other to define a channel region, a gate electrode formed over the channel region, a source region formed in contact with one of the LDD regions on an opposite side of the channel region, and a drain region formed in contact with another LDD region on an opposite side of the channel region. As recited by claim 14, each of the source region and the drain region comprises a first

impurity diffusion region including a first P-type impurity and located in the proximity of a surface of the semiconductor substrate, and a second P-type impurity diffusion region located below the first impurity diffusion region and including a second P-type impurity having a smaller diffusion coefficient in the semiconductor substrate than the first P-type impurity. Further claim 14 requires “each of the LDD regions including the first P-type impurity and not including the second P-type impurity.”

Sultan fails to teach or suggest all the limitations of claim 14. For instance, Sultan teaches that the indium implanting step is employed prior to the boron implanting step. *See* Sultan at col. 5, lines 53-55. As taught by Sultan, the indium is implanted just under the sidewall, and boron is subsequently implanted. *See* Sultan at Figs. 1e and 1f and col. 6, lines 8-10 and 44-45. Thus, the LDD region in the semiconductor taught by Sultan includes both indium and boron.

As a result, Sultan fails to teach or suggest *at least* the feature of the LDD region including the first P-type impurity and the LDD region not including the second P-type impurity. As shown in the exemplary embodiment depicted in Figure 1A, the LDD region 7 under the sidewall does not include indium (i.e., the second P-type impurity).

Accordingly, claim 14 is believed to be allowable. Further, claims 15-17 are believed to be allowable at least by virtue of depending from claim 14. Allowance of claims 14-17 is therefore requested.

Claim 18

Independent claim 18 defines a novel semiconductor device, comprising, *inter alia*, a gate electrode formed on a semiconductor substrate, a LDD region formed beside said gate electrode, the LDD region including a first P-type impurity, a sidewall formed on a lateral face of said gate electrode; a first impurity diffusion region formed beside the sidewall and in deeper position than the LDD region, the first impurity diffusion region including the first P-type impurity; and a second impurity diffusion region that is formed beside the sidewall and in further deeper position than the first impurity diffusion region, said second impurity diffusion region including a second P-type impurity that has a smaller diffusion coefficient than a first P-type impurity. In addition claim 18 requires an impurity concentration of the second impurity diffusion region is lower than that of the first impurity diffusion region, and distance between second impurity diffusion regions that are formed on both sides of the gate electrode is larger than that between first impurity diffusion regions that are formed on both sides of the gate electrode.

Applicant submits that Sultan fails to teach or suggest all the features of this claim. For example, Sultan teaches that the semiconductor device has an impurity concentration distribution of a source/drain region, such that the semiconductor device has a “double structure” which merely includes an LDD region and a source/drain region. *See* Sultan at Fig.1i and col. 8, lines 30-42. Conversely, claim 18 defines a semiconductor device including the claimed LDD region, first impurity diffusion region, and second impurity diffusion region. In an exemplary embodiment, the semiconductor device according to claim 18 has a “triple structure” comprising

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an LDD region, a source/drain region including the boron, and a source/drain region including the indium. *See* Specification at Figure 1A. Sultan clearly does not teach or suggest such a configuration.

For at least the foregoing reasons, claim 18 is believed to be allowable. Further, claims 19-21 are believed to be allowable at least by virtue of depending from claim 18. Accordingly, allowance of claims 18-21 is requested.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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